REMARKS – General

By the above requested amendment, Applicant has modified the language of the specification to help clarify the novelty of the invention.

Also applicants have rewritten all the claims to define the invention more particularly and distinctly so as to overcome the technical rejections and define the invention patentability over prior art.

Elections/Restrictions

Claim 17 is withdrawn and has been removed from the re-written claims 25 through 32.

Comments on "Response to Arguments" of Final Office Action

Page 3, 1st paragraph – Independent claim 13 has been re-written as claim 25 to incorporate the distinct features of this invention in the primary independent claim. This highlights the fact that this invention does not rely on pre-determined test data such as test vectors or test executives to provide real-time feedback on the logic state of devices under test and validates the arguments provided in Amendment A.

Page 4, 1st paragraph of Final OA – This paragraph points out that Mulrooney teaches "the host computer monitors the real-time operation of a target device having a scan chain by identifying devices connected to the scan chain, downloading from the host computer to the target device, target programs associated with the identified devices; synchronously running all of the target programs; and transmitting results data, compiled as a result of running the target programs, in real-time to the host computer without interrupting the operation of the target device (column 2 lines 38-50)." In re-written claim 25, it is clear that the present invention does not rely on downloading target programs to the target, running target programs, or receiving transmitted results data from target programs to present real-time logic states.

Page 4, paragraph 2 of Final OA – Re-written claim 25 now specifically points out that this invention does not require test vectors or test vectors to execute boundary scan tests, thereby validating the argument that the present invention is novel and patentable over the prior art.

Page 5, paragraph1 of Final OA– Examiner states: "It is unclear what the new and unexpected results of having the ability to directly monitor and control the raw boundary scan data via a graphical user interface would be." In the re-written claim 25, it is now highlighted that the present invention does not require prepared test vectors or test executives to perform boundary scan operations. Prior to this invention, users were required to prepare and generate test vectors and test executives to tell the boundary scan software how to test the target system. This is an extremely tedious and time consuming effort, and runs as a batch process providing a list of errors or potential problems when the test is complete. In contrast, the present invention doesn't rely on test vectors or test executives, so the user is up and running in seconds, not days or weeks and the results are displayed in real time, not as a batch report at the end. The real-time update feature provides the user with feedback that can be used to determine if signals are active or not. This is especially important with today's micro-miniature circuits where traditional test equipment (oscilloscopes, for example) can't be used to determine the real-time status of a signal because the integrated circuits have become so small that the test probes are now too big to be effective or in the case of the BGA packages used where circuit pins are not accessible at all.

Page 5, paragraph 2 of Final OA– Re-written claim 25 now incorporates the features listed in this paragraph which validates the argument proposed in Amendment A (the non-reliance on test vectors).

Page 6, paragraphs1,2 of Final OA – Re-written claims now include content to validate arguments and clearly point out patentable novelty.

Page 6, paragraph 3 of Final OA – This paragraph states "... it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the full graphical interpretation of boundary scan operations of JTAG Technologies with the method of Mulrooney." The "obvious" combination of these two inventions would produce an invention that specifically requires test vectors, test executives and/or target programs to function. The present invention does not have such limitations or restrictions and is therefore un-obvious and novel.

Page 7, paragraph 1 (paragraph continued from previous page) – Mulrooney teaches that feedback is provided " in order for the user to more easily understand how a test is progressing." The Mulrooney invention provides information on the progress of a test running on a target program in real-time. In contrast, the present invention provides the raw boundary scan data in real-time, not test results and does not require or rely on test programs to function as indicated by the absence of any requirements in the specification or claims.

"JTAG Technologies teaches full graphical interpretation of boundary scan operations and results .." JTAG Technologies is teaching the non-real time graphical display of test results obtained from boundary scan testing using test vectors. The present invention displays the raw boundary scan data for the user to interpret in real-time without the need for test vectors or test executives or automated interpretation (ala JTAG Technologies) of any kind. This allows the user to quickly identify which circuit signals are active, logic states of signals, continuity issues, etc all without the need for pre-determined test vectors.

Claim Rejections – 35 USC 112

Page 7, 1st paragraph – Claim 17 has been removed.

Allowable Subject Matter

Claims have been re-written to incorporate allowable subject matter identified in this section.

Claim Objections

Claim 21 has been incorporated into Claim 25. Requested correction no longer necessary.

Claim Rejections – 35 USC 103

Page 9, paragraphs 1, 2: Claims 13, and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over .S. Patent No. 6,279,123 Mulrooney in view of "JTAG Visualizer Makes Boundary Scan Visible Powerful Tool at DFT Assessment and Repair of PCB's" JTAG Technologies Press information release date November 6, 2001.

Claim 13 has been re-written as claim 25 to specifically highlight the advantages of the present invention and to describe its novelty. Specifically, combining the teachings of Mulrooney and JTAG Visualizer would produce an invention that provides real-time graphical results of tests that specifically require pre-determined test vectors, test executives and/or downloaded target programs. In contrast, the present invention graphically displays the raw boundary scan data, not test results, in real-time and does not require the use of test vectors, test executives, or test programs to display these results in real time. This provides users with the advantage of debugging target devices in real time without having to spend time (sometimes days or weeks) preparing to run the tests.

As per claim 14 (re-written as claim 26), JTAG Technologies teaches the varying of the graphics and colors of the displayed devices and the full "graphical interpretation of boundary-scan operations and results." It does not teach the

graphical representation of the raw boundary scan data in real time as identified by claim 26.

Claim 18 (page 10 of Final OA) has been deleted.

Claims 19, 20 (page 10 of Final OA) have been re-written as claims 27 and 28. Mulrooney and JTAG Technologies teach the use of graphics to display testing progress and the interpretation of boundary scan test results. The present invention teaches the use of graphics to display the raw boundary san data. For example, each pin on an integrated circuit typically has 3 boundary scan cells associated with it, one monitors the output buffer, one monitors the input buffer and one monitors the output buffer enable of the pin on the device. The present invention allows the user to monitor any or all of theses scan cells in real time to see if a signal pin on an integrated circuit is being driven from inside the part or outside the part, is enabled, is toggling or is a static high or low. These are all important considerations when doing low level debug of a circuit card and is information not provided by in this manner by any prior art.

Claim 23 has been re-written as Claim 31 (page 10 of Final OA). JTAG Technologies teach graphical representation of boundary scan operations and Mulrooney teaches displaying testing progress. Neither teaches directly or even implies the use of a graphical representation of the I/O port being used to interface to the target.

Claims 21 and 22 have been re-written as claims 29 and 30. "Mulrooney teaches that the command line parameters may be input from the configuration file or can be directly input from the keyboard of the host computer using the host control panel GUI, if the host user wishes to modify the diagnostics specified by the configuration file." Mulrooney teaches modifying the diagnostics to be run by the target program. It does not teach the direct manipulation of the raw boundary scan data of this invention. This is important because it allows the user to

directly manipulate the output buffer and buffer enable without any intervening test or diagnostic interpretation. For example – if the user simply wants to drive a signal out of an integrated circuit, the present invention allows this direct manipulation without any interference. This is especially useful when testing new prototype boards where test vectors have not been developed yet or can't be developed due to the unstable nature of the net list at this early time in the development of the circuit card.

Conclusion

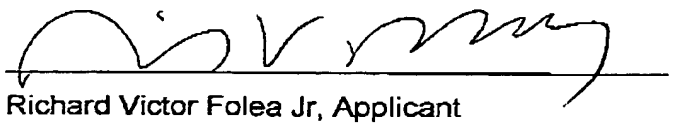
The claims have been re-written to specifically describe the unique and novel features of this invention. It is important to understand that prior art relies on prepared test vectors, test executables, test executives and/or test programs to produce test results in real time. The present invention does not require the use of these elements and provides a view of the raw boundary scan data (not test results and/or interpretations) thereby providing the user with debug tool that is simple and easy to use with minimal preparation effort and provides un-restricted access to the raw boundary scan information in real-time.

For all of the above reasons, applicant submits that the specification and claims are now in proper form, and that the claims all define patentability over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action applicant respectfully solicits.

Conditional Request For Constructive Assistance

Applicants have amended the specification and claims of this application so that they are proper, definite, and define novel structure that is also unobvious. If for any reason this application is not believed to be in full condition for allowance, applicants respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P. 2173.02 and 707.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need for further proceedings.

Very respectfully,



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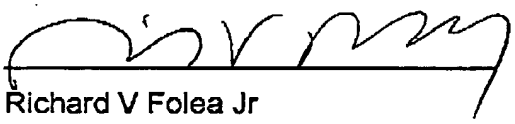

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Substance of Interview Summary, per MPEP Section 713.04

Phone Interview, 2/9/05
Examiner: Cynthia Britt, 2133

Description of exhibits or demonstrations – none

Claims Discussed – Claims 13-24 (All claims in Amendment A)

Prior Art Discussed – Mulrooney and JTAG Technologies references in 1st OA

Identification of principle amendments discussed: Amendment A

General Thrust of Principle Arguments presented to Examiner: This was primarily a review of the proposed amendment; arguments were not required for this discussion.

Other Pertinent matters Discussed: General discussions to help the examiner better understand the invention.

General Results or Outcome: Examiner made several suggestions on how to correct inconsistencies, cleanup formalities, and restructure claims to better represent the invention.